**Vector processor**

**Control signals**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **OP**  **TYPE** | **Input op\_code** | | | **Output**  **controle signal** | | | | | | |
|  | **A** | **B** | **C** | **WE\_A\_REG** | **WE\_B\_REG** | **WE\_MEM** | **MUX0** | **MUX1** | **MUX2** | **Mux3** |
| **ADD** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **1** |
| **MUL** | **0** | **0** | **1** | **1** | **0** | **0** | **0** | **0** | **1** | **1** |
|  | **0** | **1** | **0** |  |  |  |  |  |  |  |
|  | **0** | **1** | **1** |  |  |  |  |  |  |  |
| **LDR** | **1** | **0** | **0** | **0** | **1** | **0** | **X=0** | **1** | **X=0** | **0** |
| **STR** | **1** | **0** | **1** | **0** | **0** | **1** | **1** | **1** | **X=0** | **0** |
| **MOV** | **1** | **1** | **0** | **1** | **0** | **0** | **X=0** | **X=0** | **1** | **1** |
| **DPRO** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **1** |

**ADD rd,sr1,sr2 >>>> rd = sr1 + sr2**

**Mul rd,sr1,sr2 >>>> rd = sr1 \* sr2**

**LDR rd,[sr1,#imm4] >>>> rd = data\_mem[sr1+imm4]**

**STR rd,[sr1,#imm4] >>>> data\_mem[sr1+imm4] = rd**

**Mov rd,sr1 >>>> rd = sr1**

**DPRO rd,sr1,sr2 >>>> rd = sr1 . sr2**